Merging Plasmonics and Silicon Photonics Technology towards Tb/s routing in optical interconnects

Alpaslan Suna and Tolga Tekin

Technische Universität Berlin, Research Center of Microperipheric Technologies, Germany
Fraunhofer Institute for Reliability and Microintegration (IZM), Berlin, Germany
Outline

- Motivation
- PICSiP (Photonics Interconnection Layer for Converged Microsystems using System-in-Package Technology)
  - Tb/s Silicon Plasmonic Router
  - Building Blocks of the Platform
    - Design and Performance
- System Experiments
- Summary
Motivation - Bottleneck

- A key bottleneck to the realization of high-performance microelectronic systems, including SiP, is the lack of low-latency, high-bandwidth, and high density off-chip interconnects. Some of the challenges in achieving high-bandwidth chip-to-chip communication using electrical interconnects include the high losses in the substrate dielectric, reflections and impedance discontinuities, and susceptibility to crosstalk.

- Obviously, the motivation for the use of photonics to overcome these challenges and leverage low-latency and high-bandwidth communication.

- The objective is to develop a CMOS compatible underlying technology to enable next generation photonic layer within the 3D SiP towards converged microsystems.

doi: 10.1109/JSTQE.2011.2113171
Photonics Interconnection Layer for Converged Microsystems using System-in-Package Technology (PICSiP)
Towards Heterogeneous Integration

- Refine the system and application requirements
- Materials and process models for on-chip/off-chip optoelectronic elements, coupling between electrical and optical systems, optical interconnect models, semiconductor modeling. Physical design tools for integrated electrical/optical systems. To allow for the increasing complexity and interactions of PICSiP, it will be necessary to simultaneously consider digital, analog, RF, and even micro-electro-mechanical systems (MEMS) and optical components
- CMOS compatible design
- Extract the methodology guidelines
- Design Rules of CMOS compatible 3D SiP (PICSiP)
Tb/s Silicon Plasmonic Router

doi: 10.1109/PHOTONICS.2010.5698810
PLATON - Merging Plasmonics and Silicon Photonics Technology towards Tb/s routing in optical interconnects

Fiber-to-Si coupler  MUX  Waveguides  Photodiode  Si-to-DLSSP coupler  Electrical wiring  Locig IC

Si Rib Waveguides

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Si rib wg spec values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂ Box Height</td>
<td>$H_{SiO₂}$</td>
<td>2</td>
<td>μm</td>
</tr>
<tr>
<td>Si waveguide width</td>
<td>$W$</td>
<td>400</td>
<td>nm</td>
</tr>
<tr>
<td>Si waveguide height</td>
<td>$H$</td>
<td>340</td>
<td>nm</td>
</tr>
<tr>
<td>Si slab height</td>
<td>$h$</td>
<td>50</td>
<td>nm</td>
</tr>
<tr>
<td>TE Propagation losses@1550nm</td>
<td>$α_{TE}$</td>
<td>2.5</td>
<td>dB/cm</td>
</tr>
<tr>
<td>TM Propagation losses@1550nm</td>
<td>$α_{TM}$</td>
<td>2.5</td>
<td>dB/cm</td>
</tr>
<tr>
<td>TE and TM Propagation@1550nm</td>
<td>Single mode</td>
<td>Single mode</td>
<td></td>
</tr>
</tbody>
</table>

Linear loss ~ 2.5 dB/cm for TM polarization

![Graph showing optical losses vs. waveguide length]
Dielectric Loaded Surface Plasmon Waveguides (DLSPP)

A. Dereux, K. Hassan, L. Markey, J.-C. Weeber (CNRS/Université de Bourgogne)
S.I. Bozhevolnyi (University of Southern Denmark, Odense)

- **DLSPP length = 60µm**
- **SPP propagation loss ~ 6dB**
Rib Waveguide Si-to-DLSPP Coupling

- **low dependence on vertical offset value**: offset=0nm
- **optimum Si rib width** ~175nm with ~2.25dB losses: only 0.25dB power penalty for Si width=400nm
- Only 0.5dB penalty compared to the strip Si-to-DLSPP coupling structure
**TM Grating Coupler**

**Shallow etched** grating coupler:
- efficiency = -4.4 dB,
- 3dB bandwidth ~ 50 nm
- period = 0.73 µm,
- etch depth = 0.14 µm,
- filling factor = 0.5,
- incidence angle = 7°

**Fully etched** grating coupler:
- efficiency = -2.68 dB,
- 3dB bandwidth ~ 55 nm
- period = 0.7 µm,
- etch depth = 0.29 µm,
- filling factor = 0.8,
- incidence angle = 10°
TM Grating Coupler

Measurements

- Simulation results for filling factor not equal to 0.5: 2.68 dB loss
- 3dB bandwidth > 50 nm

![Graph showing fiber-to-fiber losses for 690, 700, and 710 nm period gratings.](image)

- Fully etched TM GC
  4.5 dB coupling losses
Detection Schemes for $\lambda=1550\text{nm}$ on SOI

- **two photon absorption in Si**
  - Non-linear effect
  - $\Rightarrow$ high intensity required

- **direct absorption in Ge or III/V material**
  - Linear effect, but requires hybrid integration
  - $\Rightarrow$ complex fabrication process

- **direct absorption at defect states**
  - Linear effect, lower spec. absorption
  - $\Rightarrow$ best compromise for simple integration and low-rate detection
Si-implanted Photodiodes

Fabricated devices with
✓ Dark current = 100 nA
✓ Bandwidth = 1 GHz
✓ Responsivity = 0.1 A/W
Thermo-optically tunable ring structures
- resonance tuning up to 2.4nm required:
- within the 3nm limit of electrically wavelength tunable silicon rings
- several structures designed for tuning spectral window operation within 1530-1560nm
Tunable Ring Resonator Structure

Parameter | Ring radius (R) | Bus-to-ring (B2R) gaps (gap₁) | Ring-to-ring (R2R) gaps (gap₂)
--- | --- | --- | ---
1:1 | 5.4 | 0.19, 0.2, 0.21 | 0.44, 0.46, 0.48 |
 | 9 | 0.19, 0.2, 0.21 | 0.36, 0.38, 0.4 |
 | 12 | 0.16, 0.17, 0.18 | 0.28, 0.3, 0.32 |
 | 14.85 | 0.165, 0.17, 0.175 | 0.26, 0.28, 0.3 |
2:1 | 5.4 | 0.19, 0.2, 0.21 | 0.44, 0.46, 0.48 |
4:1 | 5.4 | 0.19, 0.2, 0.21 | 0.44, 0.46, 0.48 |
Spectral Response of Ring Resonator

Spectral response of 1:1 fabricated devices

Static characterization

- $R = 5.4 \, \mu m$  $FSR = \sim 15.4 \, nm$
- $R = 9 \, \mu m$  $FSR = \sim 9.25 \, nm$
- $R = 12 \, \mu m$  $FSR = \sim 6.9 \, nm$
- $R = 14.85 \, \mu m$  $FSR = \sim 5.6 \, nm$
Spectral Response of Ring Resonator

Spectral response of 1:1 fabricated devices

Thermo-optical characterization
MUX based on 2nd order Ring Resonator

Spectral response of the fabricated designs

Table with specifications of the fabricated ring structures, simulation parameters of their models, and the matching results.

![Spectral response graphs](image)

Figure 6.19: Spectral responses of the a) first (1534-1540 nm band), b) second (1540-1547 nm band), c) third (1547-1554 nm band) and d) fourth (1557-1563 nm band) 8:1 multiplexing designs.
DLSPP switches on SOI platform
Control ASIC

- FPGA for 4x4 works in simulation & FPGA
- FPGA-to-ASIC conversion is finished and Gate-level simulation works
ASIC for 4x4 Router

- Header detection in RTL-simulation shows successful performance
- Header detection in gate-level simulation shows gate delay – optimization needed (on-going)
- First chips received
First Transmission Experiment on DLSPP

- Si length = 5mm
- DLSPP length = 60µm
- Si – fiber loss ~ 24dB
- Si propagation loss ~ 2.3dB
- Si – DLSPP losses ~ 5.3dB
- SPP propagation loss ~ 6dB
- OOK
- NRZ coding
- 10Gbps BER
Plasmonic Device at 0.480 Tb/s Demonstrated

Fig. 1. (a) 480Gb/s WDM Experimental Setup, (b) Channel Spectrum before entering the chip, (c) Channel Spectrum directly at the chip’s output and Measured Spectral Response of the SOI – Plasmonic chip, (d) Channel Spectrum after being amplified in the receiver’s EDFA.

Fig. 2. (a) BER curves for all 40Gb/s B2B and transmitted channels, and BER curves and Eye Diagrams for (b) channel #1 (Best – Performing Channel) and (c) channel #8 (Worst – Performing Channel).

http://www.opticsinfobase.org/oe/abstract.cfm?URI=oe-20-7-7655

© Fraunhofer IZM ITG Workshop, microsys berlin, 20.03.2012
Active Plasmonics in True Data Traffic Applications: Thermo-optic ON/OFF Gating using a Si-Plasmonic Asymmetric MZI

2.8 μs response time and 10.8 mW power consumption


doi: 10.1109/LPT.2011.2177964
Summary

✓ Photonic integrated System-in-Package platform for Tb/s Silicon-Plasmonic router has been presented, first implementation of PICSiP concept
✓ Building blocks have been designed, fabricated and performances demonstrated
✓ Furthermore first system experiments reported using the building blocks of the platform

We are confident of applicability of PLATON concepts in real High Productivity Computing Systems (HPCS) interconnects

✓ Tb/s throughput
✓ 40Gb/s per input
✓ 280Gb/s per output port
✓ ~5W power consumption
✓ 6” wafer size
✓ psec latency
Acknowledgements

This work has been partly supported by the European FP7

**PLATON** - Merging Plasmonic and Silicon Photonics Technology towards Tb/s routing in optical interconnects, Contract Number 249135

- Nikos Pleros, S. Papaioannou, K. Vyrsokinos, O. Tsilipakos, A. Pitilakis, Emmanouil Kriezisc (CERTH/Aristotle University of Thessaloniki)
- A. Dereux, K. Hassan, L. Markey, J.-C. Weeber (CNRS/Université de Bourgogne)
- S.I. Bozhevolnyi (University of Southern Denmark, Odense)
- M. Waldow, Matthias Baus, Matthias Karl (AMO GmbH, Aachen)
- H. Avramopoulos, D. Kalavrouziotis, G. Giannoulis (National Technical University of Athens)
- Oriol Gili de Villasante, Paul Tcheg, Bei Wang, Sascha Lutzmann, Bouchaib Bouhlal (Fraunhofer IZM and TU-Berlin)